

PowerPC™

Implementation Variances Relative to Rev. 1 of *The Programming Environments Manual*

This document describes variances between each PowerPC processor and the information provided in *PowerPC Microprocessor Family: The Programming Environments*, Rev 1, referred to as *The Programming Environments Manual*. For more information about individual PowerPC implementations, see the user's manual for the appropriate processor. Some of these variances occurred with *The Programming Environments Manual*, Rev. 0.1. The column labeled 'PEM Revision' in each table identifies the revision levels of *The Programming Environments Manual* from which the processor varies.

In this document, the terms '603', '603e', '604', and '604e' are abbreviations for 'PowerPC 603 microprocessor', 'PowerPC 603e microprocessor', 'PowerPC 604 microprocessor', and 'PowerPC 604e microprocessor', respectively.

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Part 1: PowerPC 603/603e Processor Family Variances

Table 1 describes the differences between the PowerPC 603™ and PowerPC 603e™ family of processors and *The Programming Environments Manual*.

Table 1. Variances for the PowerPC 603 and 603e Processors

Variance	Processor	Notes	PEM Revision
The PowerPC 603e processor does not implement the direct-store facility. The 603e does not implement the SR[T] bit or the direct-store exceptions conditions.	603e	—	Rev. 0.1 Rev. 1
The architecture allows data accesses from more than one instruction to be combined for cache-inhibited operations except when the accesses are separated by a sync instruction, or by an eieio instruction when the page or block is also designated as guarded. This combined access capability is not implemented on the 603- and 603e-based processors.	603, 603e	Store operations with write-through attributes may cause any part of valid data in the cache to be written back to main memory.	Rev. 0.1 Rev. 1
The architecture no longer permits DSISR bits 0 and 5 to be set simultaneously. This is however permitted in 603- and 603e-based processors.	603, 603e	—	Rev. 0.1 Rev. 1

Part 2: PowerPC 604/604e Processor Family Variances

Table 2 lists the variances between the PowerPC 604™ and PowerPC 604e™ processors and *The Programming Environments Manual*.

Table 2. Variances for the PowerPC 604/604e Processors

Variance	Processor	Notes	PEM Revision
The 604 (Rev. 3.5) does not ensure that dcbf and loads are ordered. Instead, the 604 places dcbf in the store queue and treats it as a store, but ignores the address compare that prevents load/store reordering. If another processor modifies a shared cache block in memory for which M = 0 and that has been cached locally as unmodified, and a dcbf instruction is executed to that cache block followed by a load to that block but the load goes ahead of the dcbf operation, the load sees the stale data in the cache. This occurs only when M = 0; with M = 1, snooping cleans any stale data in the cache.	604 (Rev. 3.5 only)	—	Rev. 0.1 Rev. 1

PRELIMINARY

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